TEXAS INSTRUMENTS

OPA189, OPA2189, OPA4189

SBOS830 – JUNE 2017

OPAx189, Precision, 36-V, 14-MHz, MUX-Friendly Low-Noise, Rail-to-Rail Output, Zero-Drift Operational Amplifiers

ADVANCE INFORMATION

1 Features

- Ultra-High Precision:
  - Ultra-Low Offset Voltage: 0.4 μV
  - Zero-Drift: 0.0035 μV/°C
- Excellent DC Precision:
  - CMRR: 168 dB
  - Open-Loop Gain: 170 dB
- Low Noise:
  - V_N at 1 kHz: 5.8 nV/$\sqrt{Hz}$
  - 0.1-Hz to 10-Hz Noise: 110 nV_{PP}
- Excellent Dynamic Performance:
  - Gain Bandwidth: 14 MHz
  - Slew Rate: 20 V/μs
  - Fast Settling: 10-V, 0.01% in 1.5 μs
- Robust Design:
  - MUX-Friendly Inputs
  - RFI/EMI Filtered Inputs
- Wide Supply Range: 4.5 V to 36 V
- Quiescent Current: 1.7 mA (Maximum)
- Rail-to-Rail Output
- Input Includes Negative Rail

2 Applications

- Precision Multi-Chanel Systems
- Bridge Amplifier
- Strain Gauges
- Temperature Measurement
- Resistance Temperature Detectors

3 Description

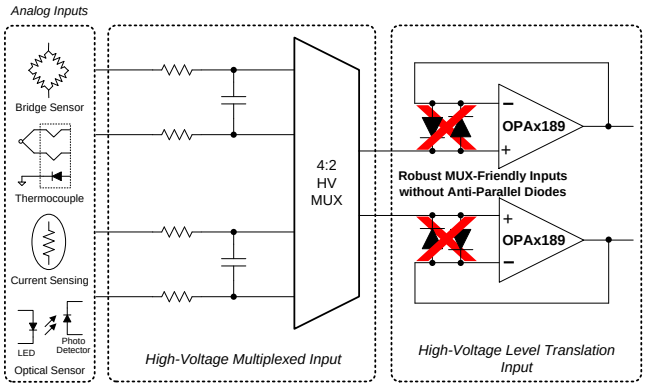
The OPAx189 (OPA189, OPA2189, and OPA4189) series of high-precision operational amplifiers are ultra-low noise, fast-settling, zero-drift devices that provide rail-to-rail output operation and feature a unique MUX-friendly architecture. These features and excellent ac performance, combined with only 0.4 μV of offset and 0.0035 μV/°C of drift over temperature, makes the OPAx189 well-suited for precision instrumentation, signal measurement, and active filtering applications. Moreover, the MUX-friendly input architecture prevents inrush current when applying large differential voltages which improves settling performance in multi-channel systems, all while providing robust ESD protection during shipment, handling, and assembly. All versions are specified from –40°C to +125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA189	SOIC (8)	4.90 mm × 3.90 mm
	SOT-23 (5)	2.90 mm × 1.60 mm
	VSSOP (8)	3.00 mm × 3.00 mm
OPA2189	SOIC (8)	4.90 mm × 3.90 mm
	VSSOP (8)	3.00 mm × 3.00 mm
OPA4189	SOIC (14)	8.65 mm × 3.90 mm
	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

OPAx189 Preserves R-C Settling Performance in a Switched or Multiplexed Application



OPAx189 MUX-Friendly Input Settles Quickly and Maintains High Input Impedance When Switched

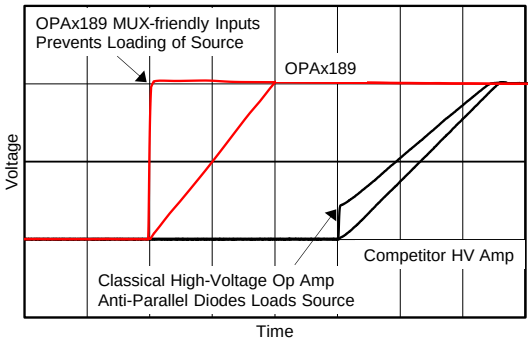


Table of Contents

ADVANCE INFORMATION

4 Revision History

DATE	REVISION	NOTES
June 2017	*	Initial release.

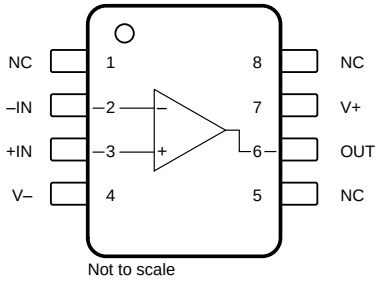
5 Device Comparison Table

FEATURES	PRODUCT
25-µV, 0.085-µV/°C, 8.8-nV/√Hz, Rail-to-Rail Output, 36-V, Zero-Drift CMOS	OPA188
5-µV, 0.05-µV/°C, 7-nV/√Hz, 10-MHz, *True* Rail-to-Rail Input/Output, 5.5-V, Zero-Drift CMOS	OPA388
10-µV, 0.05-µV/°C, 25-µA, Rail-to-Rail Input/Output, 5.5-V, Zero-Drift CMOS	OPA333
25-µV, 0.8-µV/°C, 140-µA, 2.5-MHz, Rail-to-Rail Input/Output, 36-V, e-Trim CMOS	OPA191
120-µV, 10-MHz, 5.1-nV/√Hz, 36-V JFET Input Industrial Op Amp	OPA140
2.2-nV/√Hz, 150-µV, 18-MHz, 36-V Bipolar Op Amp in SOT-23 package	OPA209

ADVANCE INFORMATION

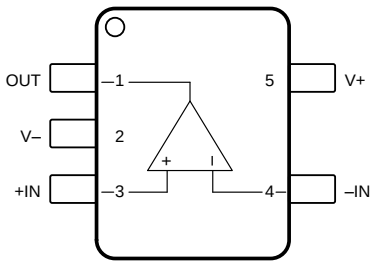
6 Pin Configuration and Functions

OPA189 D and DGK Packages
8-Pin SOIC, 8-Pin VSSOP
Top View



Not to scale

OPA189 DBV Package
5-Pin SOT-23
Top View



Not to scale

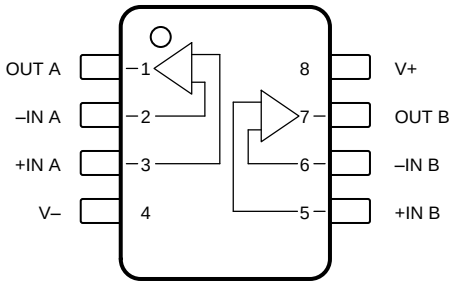
NC - No internal connection.

Pin Functions: OPA189

PIN			I/O	DESCRIPTION
NAME	OPA189			
	D (SOIC) DGK (VSSOP)	DBV (SOT-23)		
–IN	2	4	I	Inverting input
+IN	3	3	I	Noninverting input
NC	1, 5, 8	—	—	No internal connection (can be left floating)
OUT	6	1	O	Output
V–	4	2	—	Negative (lowest) power supply
V+	7	5	—	Positive (highest) power supply

ADVANCE INFORMATION

OPA2189 D and DGK Packages
8-Pin SOIC, 8-Pin VSSOP
Top View



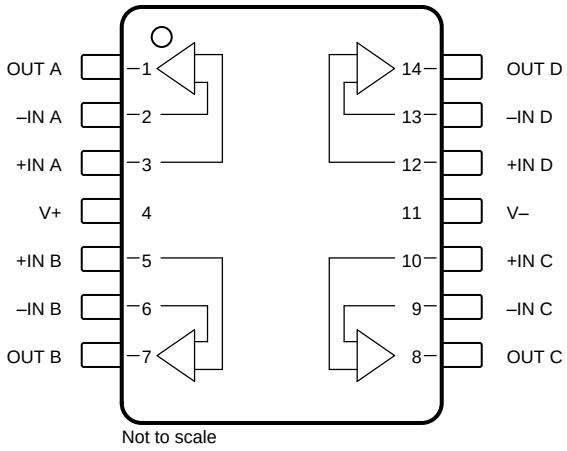
Not to scale

Pin Functions: OPA2189

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input channel A
+IN A	3	I	Noninverting input channel A
–IN B	6	I	Inverting input channel B
+IN B	5	I	Noninverting input channel B
OUT A	1	O	Output channel A
OUT B	7	O	Output channel B
V–	4	—	Negative supply
V+	8	—	Positive supply

ADVANCE INFORMATION

OPA4189 D and PW Packages
14-Pin SOIC, 14-Pin TSSOP
Top View



Not to scale

NC - No internal connection.

Pin Functions: OPA4189

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input channel A
+IN A	3	I	Noninverting input channel A
–IN B	6	I	Inverting input channel B
+IN B	5	I	Noninverting input channel B
–IN C	9	I	Inverting input channel C
+IN C	10	I	Noninverting input channel C
–IN D	13	I	Inverting input channel D
+IN D	12	I	Noninverting input channel D
OUT A	1	O	Output channel A
OUT B	7	O	Output channel B
OUT C	8	O	Output channel C
OUT D	14	O	Output channel D
V–	11	—	Negative supply
V+	4	—	Positive supply
NC	—	—	No internal connection (can be left floating)

ADVANCE INFORMATION

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Supply voltage	V_S = (V+) – (V–)	Single-supply		40	V
		Dual-supply		±20	
Signal input pins	Voltage	Common-mode	(V–) – 0.5	(V+) + 0.5	
		Differential		(V+) – (V–) + 0.2	
	Current			±10	mA
Output short circuit(2)			Continuous	Continuous	
Temperature	Operating, T_A		–55	150	°C
	Junction, T_J			150	
	Storage, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)	Single-supply	4.5		36	V
	Dual-supply	±2.25		±18	
Specified temperature		–40		125	°C

ADVANCE INFORMATION

7.4 Thermal Information: OPA189

THERMAL METRIC(1)		OPA189			UNIT
		D (SOIC)	DGK (VSSOP)	DBV (SOT)	
		8 PINS	8 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	136	143	205	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	74	47	200	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62	64	113	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19.7	5.3	38.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	54.8	62.8	104.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Thermal Information: OPA2189

THERMAL METRIC(1)		OPA2189		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	136	143	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	74	47	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62	64	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19.7	5.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	54.8	62.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.6 Thermal Information: OPA4189

THERMAL METRIC(1)		OPA4189		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86	93	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46	28	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41	34	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	11.3	1.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	40.7	33.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

ADVANCE INFORMATION

7.7 Electrical Characteristics

at T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±0.4	±2.5	µV
		T_A = –40°C to 125°C				±4.5	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to 125°C			±0.0035	±0.02	µV/°C
PSRR	Power-supply rejection ratio	T_A = –40°C to 125°C			±0.005	±0.05	µV/V
INPUT BIAS CURRENT							
I_B	Input bias current	R_{IN} = 100 kΩ			±70	±300	pA
			T_A = –20°C to 85°C			±400	
			T_A = –40°C to 125°C			±600	
I_{OS}	Input offset current				±140	±600	
			T_A = –20°C to 85°C			±800	
			T_A = –40°C to 125°C			±1200	
NOISE							
E_N	Input voltage noise	f = 0.1 Hz to 10 Hz			17		nV_{RMS}
					0.11		$µV_{PP}$
e_N	Input voltage noise density	f = 10 Hz			5.8		nV/√Hz
		f = 100 Hz			5.8		
		f = 1 kHz			5.8		
		f = 10 kHz			5.8		
I_N	Input current noise density	f = 1 kHz			165		fA/rtHz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range			(V–) – 0.1		(V+) – 2.5	V
CMRR	Common-mode rejection ratio	(V–) – 0.1 V ≤ V_{CM} ≤ (V+) – 2.5 V	V_S = ±2.25 V	120	140		dB
			V_S = ±18 V	146	168		
		(V–) – 0.1 V ≤ V_{CM} ≤ (V+) – 2.5 V, T_A = –40°C to 125°C	V_S = ±18 V	144	156		
			V_S = ±2.25 V	116	130		
INPUT IMPEDANCE							
z_{id}	Differential input impedance				100 || 2		MΩ || pF
z_{ic}	Common-mode input impedance				60 || 4		TΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = ±18 V, (V–) + 0.3 V < V_O < (V+) – 0.3 V, R_{LOAD} = 10 kΩ		150	170		dB
		V_S = ±18 V, (V–) + 0.3 V < V_O < (V+) – 0.3 V, R_{LOAD} = 10 kΩ, T_A = –40°C to 125°C		130	160		
		V_S = ±18 V, (V–) + 0.6 V < V_O < (V+) – 0.6 V, R_{LOAD} = 2 kΩ		150	170		
		V_S = ±18 V, (V–) + 0.6 V < V_O < (V+) – 0.6 V, R_{LOAD} = 2 kΩ, T_A = –40°C to 125°C		130	160		

ADVANCE INFORMATION

Electrical Characteristics (continued)

at T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Gain-bandwith Product	A_V = 1000			14		MHz
UGB	Unity-gain Bandwith	A_V = 1			9		MHz
SR	Slew rate	G = 1, 10-V step			20		V/µs
THD+N	Total harmonic distortion + noise	G = 1, f = 1 kHz, V_O = 3.5 V_{RMS}			0.0001%		
t_S	Settling time	To 0.1%	V_S = ±18 V, G = 1, 10-V step		0.5		µs
		To 0.01%	V_S = ±18 V, G = 1, 10-V step		1.5		µs
t_{OR}	Overload recovery time	V_{IN} × G = V_S			400		ns
OUTPUT							
V_O	Voltage output swing from rail	Positive rail	No load		5	15	mV
			R_{LOAD} = 10 kΩ		20	110	mV
			R_{LOAD} = 2 kΩ		80	500	mV
		Negative rail	No load		5	15	mV
			R_{LOAD} = 10 kΩ		20	110	mV
			R_{LOAD} = 2 kΩ		80	500	mV
		T_A = –40°C to 125°C, both rails, R_{LOAD} = 10 kΩ			20	110	mV
I_{SC}	Short-circuit current				±65		mA
C_{LOAD}	Capacitive load drive						
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A			100		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	V_S = ±2.25 V (V_S = 4.5 V)	I_O = 0 A		1.3	1.7	mA
			T_A = –40°C to 125°C, I_O = 0 A		1.3	1.8	mA
		V_S = ±18 V (V_S = 36 V)	I_O = 0 A		1.3	1.7	mA
			T_A = –40°C to 125°C, I_O = 0 A		1.3	1.8	mA
TEMPERATURE							
T_A	Specified range			–40		125	°C
V_S	Specified supply voltage range			4.5 (±2.25)		36 (±18)	V

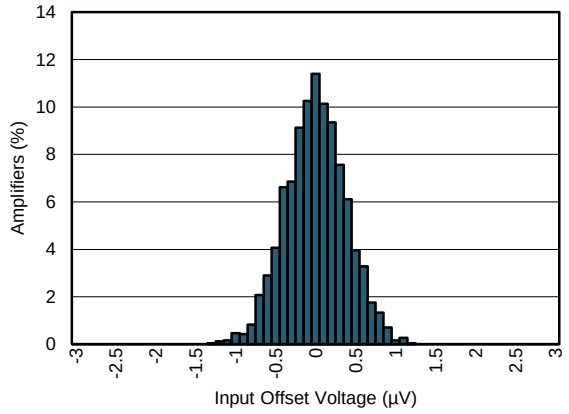
ADVANCE INFORMATION

7.8 Typical Characteristics

Table 1. Typical Characteristic Graphs

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	Figure 1
Offset Voltage Drift Distribution	Figure 2

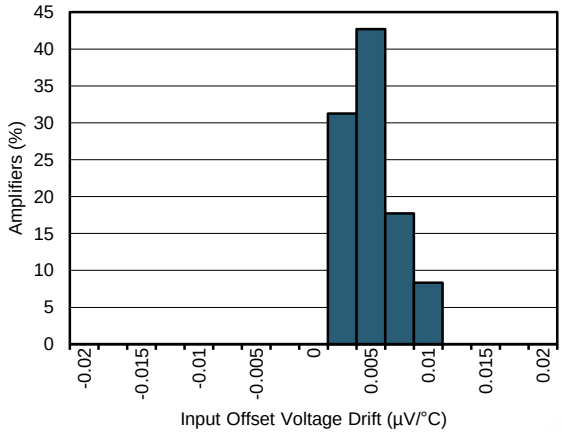
at V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



µ = 46.67 nV σ = 374.5 nV N = 2554

V_{OS} (maximum) = ±2.5 µV

Figure 1. Offset Voltage Production Distribution



µ = 3.79 nV/°C σ = 2.11 nV/°C N = 96

dV_{OS} / dT (maximum) = ±0.02 µV/°C

Figure 2. Offset Voltage Drift Distribution

ADVANCE INFORMATION

8 Detailed Description

8.1 Overview

The OPAx189 operational amplifier combines precision offset and drift with excellent overall performance, making the device well-suited for many precision applications. The precision offset drift of only 0.0035 µV/°C provides stability over the entire temperature range. In addition, this device offers excellent linear performance with high CMRR, PSRR, and A_{OL}. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate. See *Layout Guidelines* for details and layout example.

The OPAx189 is part of a family of zero-drift, MUX-friendly, rail-to-rail output operational amplifiers. These devices operate from 4.5 V to 36 V, are unity-gain stable, and are suitable for a wide range of general-purpose and precision applications. The zero-drift architecture provides ultra-low input offset voltage and near-zero input offset voltage drift over temperature and time. This choice of architecture also offers outstanding ac performance, such as ultra-low broadband noise, zero flicker noise, and outstanding distortion performance when operating below the chopper frequency.

8.2 Functional Block Diagram

Figure 3 shows a representation of the proprietary OPAx189 architecture.

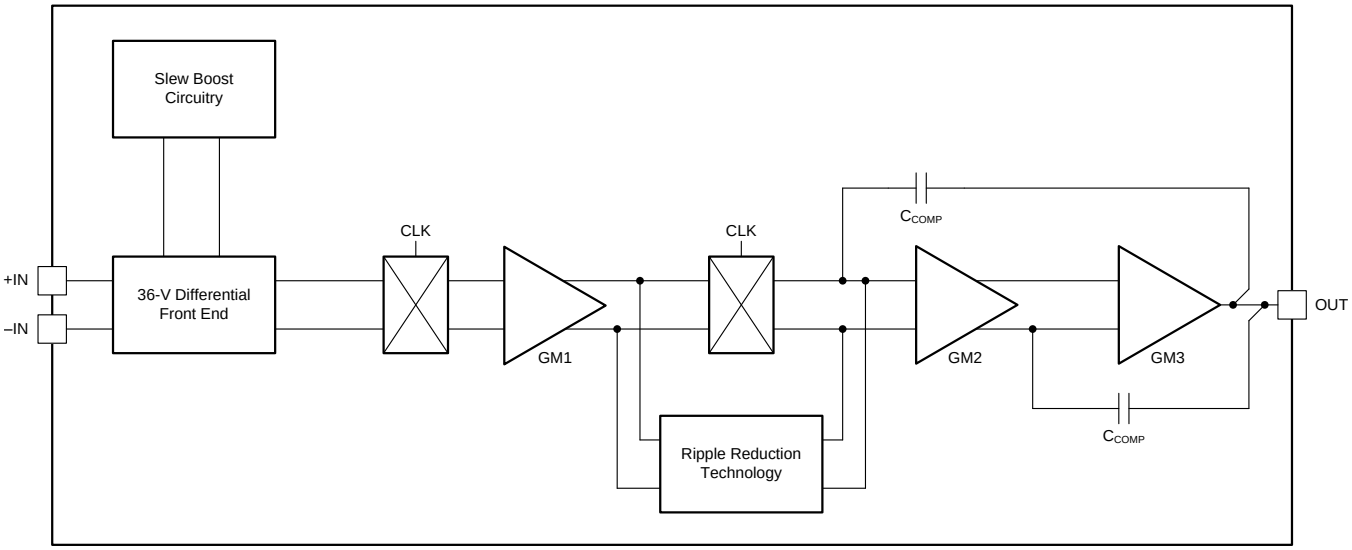


Figure 3. Functional Block Diagram

8.3 Feature Description

The OPA189, OPA2189, and OPA4189 series of op amps can be used with single or dual supplies from an operating range of V_S = 4.5 V (±2.25 V) up to V_S = 36 V (±18 V). These devices do not require symmetrical supplies; they only require a minimum supply voltage of 4.5 V (±2.25 V). For V_S less than ±2.5 V, the common-mode input range does not include midsupply. Supply voltages higher than 40 V can permanently damage the device; see the *Absolute Maximum Ratings* table for details. Key parameters are given over the specified temperature range, T_A = –40°C to +125°C, in *Electrical Characteristics*. Key parameters that vary over the supply voltage, temperature range, or frequency are shown in *Typical Characteristics*.

The OPAx189 is unity-gain stable and free from unexpected output phase reversal. This device uses a proprietary, periodic autocalibration technique to provide low input offset voltage and very low input offset voltage drift over time and temperature. For lowest offset voltage and precision performance, optimize circuit layout and mechanical conditions. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. Cancel these thermally-generated potentials by ensuring they are equal on both input pins. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat sources.
- Shield operational amplifier and input circuitry from air currents, such as cooling fans.

Follow these guidelines to reduce the likelihood of junctions being at different temperatures, which may cause thermoelectric voltages of 0.1 µV/°C or higher, depending on the materials used. See *Layout Guidelines* for details and layout example.

8.3.1 Operating Characteristics

The OPAx189 is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V). Many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

8.3.2 Phase-Reversal Protection

The OPAx189 has an internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPAx189 input prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. This performance is shown in Figure 4.

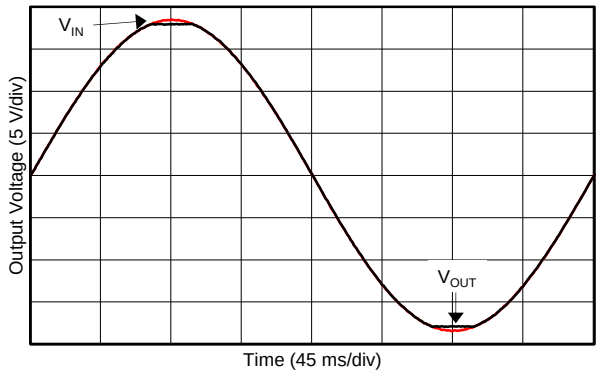


Figure 4. No Phase Reversal

ADVANCE INFORMATION

Feature Description (continued)

8.3.3 Input Bias Current Clock Feedthrough

Zero-drift amplifiers such as the OPAx189 use switching on the inputs to correct for the intrinsic offset and drift of the amplifier. Charge injection from the integrated switches on the inputs can introduce short transients in the input bias current of the amplifier. The extremely short duration of these pulses prevents the pulses from amplifying, however the pulses may be coupled to the output of the amplifier through the feedback network. The most effective method to prevent transients in the input bias current from producing additional noise at the amplifier output is to use a low-pass filter such as an RC network.

8.3.4 EMI Rejection

The OPAx189 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI interference from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx189 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. Figure 5 shows the results of this testing on the OPAx189. Table 2 lists the EMIRR IN+ values for the OPAx189 at particular frequencies commonly encountered in real-world applications. Applications listed in Table 2 may be centered on or operated near the particular frequency shown. Detailed information can also be found in *EMI Rejection Ratio of Operational Amplifiers* (SBOA128), available for download from www.ti.com.

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many op amps is a change in the offset voltage as a result of RF signal rectification. An op amp that is more efficient at rejecting this change in offset as a result of EMI has a higher EMIRR and is quantified by a decibel value. Measuring EMIRR can be performed in many ways, but this section provides the EMIRR IN+, which specifically describes the EMIRR performance when the RF signal is applied to the noninverting input pin of the op amp. In general, only the noninverting input is tested for EMIRR for the following three reasons:

- Op amp input pins are known to be the most sensitive to EMI, and typically rectify RF signals better than the supply or output pins.
- The noninverting and inverting op amp inputs have symmetrical physical layouts and exhibit nearly matching EMIRR performance
- EMIRR is more simple to measure on noninverting pins than on other pins because the noninverting input terminal can be isolated on a PCB. This isolation allows the RF signal to be applied directly to the noninverting input terminal with no complex interactions from other components or connecting PCB traces.

High-frequency signals conducted or radiated to any pin of the operational amplifier may result in adverse effects, as the amplifier would not have sufficient loop gain to correct for signals with spectral content outside the bandwidth. Conducted or radiated EMI on inputs, power supply, or output may result in unexpected DC offsets, transient voltages, or other unknown behavior. Take care to properly shield and isolate sensitive analog nodes from noisy radio signals and digital clocks and interfaces.

The EMIRR IN+ of the OPAx189 is plotted versus frequency as shown in Figure 5. If available, any dual and quad op amp device versions have nearly similar EMIRR IN+ performance. The OPAx189 unity-gain bandwidth is 14 MHz. EMIRR performance below this frequency denotes interfering signals that fall within the op amp bandwidth.

Feature Description (continued)

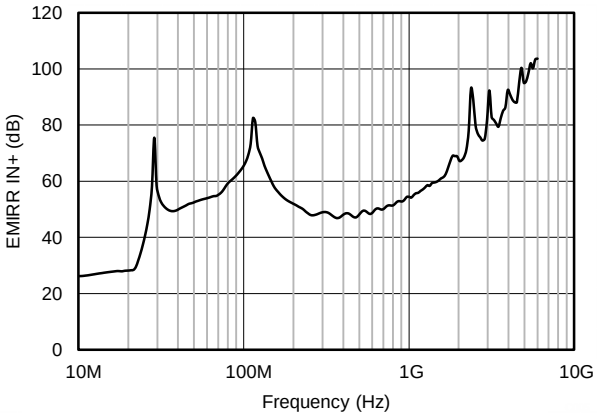


Figure 5. EMIRR Testing

Table 2. OPAx189 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION AND ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	48.4 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	52.8 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	69.1 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	88.9 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	82.5 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	95.5 dB

8.3.5 EMIRR +IN Test Configuration

Figure 6 shows the circuit configuration for testing the EMIRR IN+. An RF source is connected to the op amp noninverting input terminal using a transmission line. The op amp is configured in a unity-gain buffer topology with the output connected to a low-pass filter (LPF) and a digital multimeter (DMM). A large impedance mismatch at the op amp input causes a voltage reflection; however, this effect is characterized and accounted for when determining the EMIRR IN+. The multimeter samples and measures the resulting DC offset voltage. The LPF isolates the multimeter from residual RF signals that may interfere with multimeter accuracy.

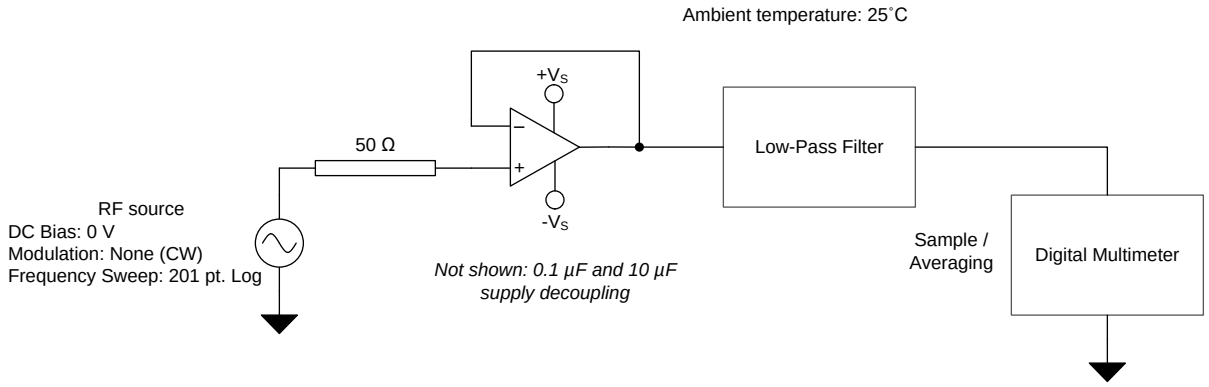


Figure 6. EMIRR +IN Test Configuration

ADVANCE INFORMATION

8.3.6 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. See Figure 7 for an illustration of the ESD circuits contained in the OPAx189 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse while discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger or threshold voltage that is above the normal operating voltage of the OPAx189 but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

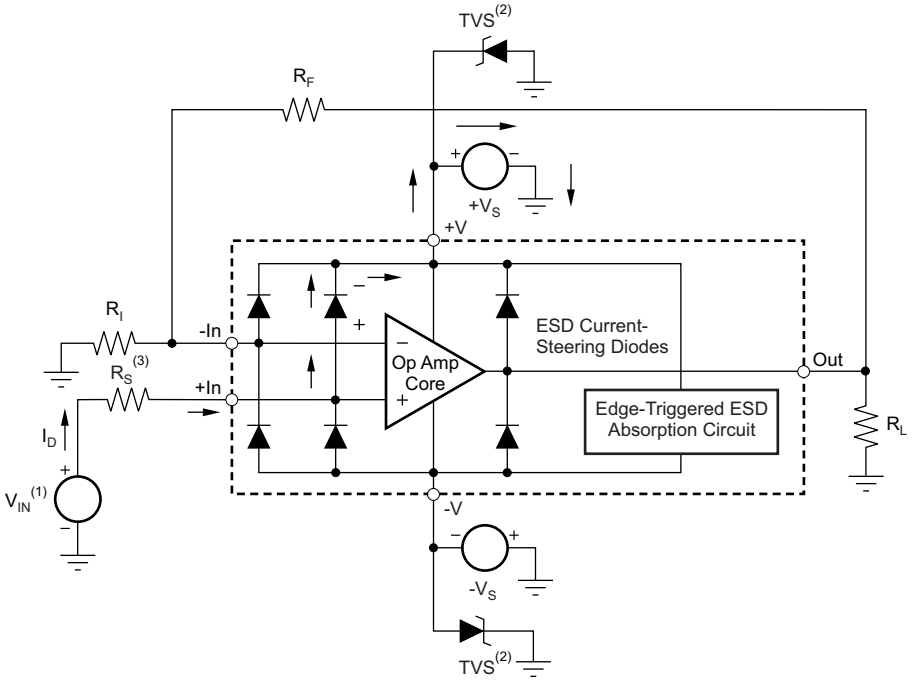
When the operational amplifier connects into a circuit (as shown in Figure 7), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

Figure 7 shows a specific example where the input voltage(V_{IN}) exceeds the positive supply voltage ($+V_S$) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ or $–V_S$ are at 0 V. Again, this question depends on the supply characteristic while at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source through the current-steering diodes. This state is not a normal bias condition; the amplifier most likely does not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, external zener diodes must be added to the supply pins, as shown in Figure 7. The zener voltage must be selected such that the diode does not turn on during normal operation. However, the zener voltage must be low enough so that the zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.



(1) $V_{IN} = +V_S + 500$ mV.

(2) TVS: $+V_{S(max)} > V_{TVSBR\ (min)} > +V_S$.

(3) Suggested value is approximately 5 kΩ.

Figure 7. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

8.3.7 MUX-Friendly Inputs

The OPAx189 features a proprietary input stage design that allows an input differential voltage to be applied while maintaining high input impedance. Typically, high-voltage CMOS or bipolar-junction input amplifiers feature anti-parallel diodes that protect input transistors from large V_{GS} voltages that may exceed the semiconductor process maximum and permanently damage the device. Large V_{GS} voltages can be forced when applying a large input step, switching between channels, or attempting to use the amplifier as a comparator.

OPAx189 solves these problems with a switched-input technique which prevents large input bias currents when large differential voltages are applied. This solves many issues seen in switched or multiplexed applications, where large disruptions to RC filtering networks are caused by fast switching between large potentials. OPAx189 offers outstanding settling performance due to these design innovations and built-in slew rate boost and wide bandwidth. The OPAx189 can also be used as a comparator. Differential and common-mode *Absolute Maximum Ratings* still apply relative to the power supplies.

ADVANCE INFORMATION

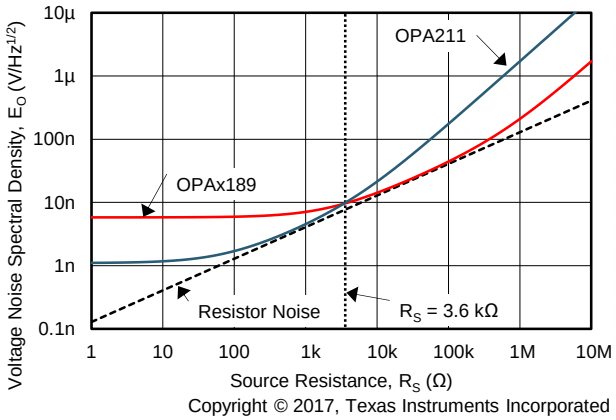
8.4 Noise Performance

Figure 8 shows the total circuit noise for varying source impedances with the operational amplifier in a unity-gain configuration (with no feedback resistor network and therefore no additional noise contributions). The OPAx189 and OPA211 are shown with total circuit noise calculated. The op amp itself contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Therefore, the lowest noise op amp for a given application depends on the source impedance. For low source impedance, current noise is negligible, and voltage noise generally dominates. The OPA189, OPA2189, and OPA4189 family has both low voltage noise and low current noise because of the CMOS input of the op amp. As a result, the current noise contribution of the OPAx189 series is negligible for any practical source impedance, which makes this device the better choice for applications with high source impedance.

The equation in Figure 8 shows the calculation of the total circuit noise, with these parameters:

- e_n = voltage noise
- I_n = current noise
- R_S = source impedance
- k = Boltzmann's constant = 1.38×10^{-23} J/K
- T = temperature in degrees Kelvin (K)

For more details on calculating noise, see *Basic Noise Calculations*.



R_S = 3.6 kΩ is indicated in Figure 8.

This is the source impedance above which OPAx189 is a lower noise option than the OPA211.

Figure 8. Noise Performance of the OPAx189 and OPA211 in Unity-Gain Buffer Configuration

8.5 Basic Noise Calculations

Low-noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases; consider the effect of source resistance on overall op amp noise performance. Total noise of the circuit is the root-sum-square combination of all noise components.

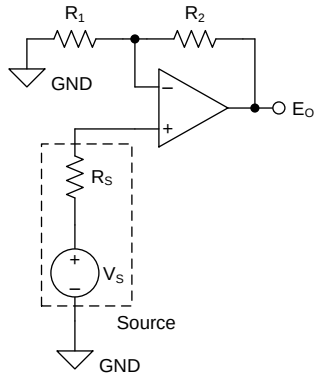
The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is plotted in Figure 8. The source impedance is usually fixed; consequently, select the op amp and the feedback resistors to minimize the respective contributions to the total noise.

Figure 9 illustrates both noninverting **(A)** and inverting **(B)** op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. In general, the current noise of the op amp reacts with the feedback resistors to create additional noise components. However, the extremely low current noise of the OPAx189 means that the current noise contribution can be neglected.

The feedback resistor values can generally be chosen to make these noise sources negligible. Low impedance feedback resistors load the output of the amplifier. The equations for total noise are shown for both configurations.

Basic Noise Calculations (continued)

(A) Noise in Noninverting Gain Configuration



Noise at the output is given as E_O, where

$$(1)\quad E_O = \left(1+\frac{R_2}{R_1}\right)\cdot\sqrt{(e_S)^2+(e_N)^2+\left(e_{R_1\|R_2}\right)^2+(i_N\cdot R_S)^2+\left(i_N\cdot\left[\frac{R_1\cdot R_2}{R_1+R_2}\right]\right)^2}\quad [\,V_{RMS}\,]$$

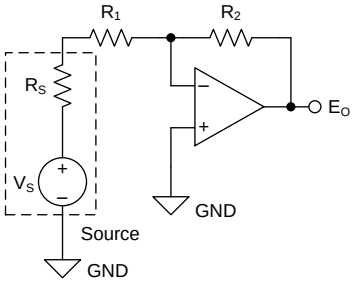
$$(2)\quad e_S = \sqrt{4\cdot k_B\cdot T(K)\cdot R_S}\quad \left[\frac{V}{\sqrt{Hz}}\right]$$ Thermal noise of R_S

$$(3)\quad e_{R_1\|R_2} = \sqrt{4\cdot k_B\cdot T(K)\cdot\left[\frac{R_1\cdot R_2}{R_1+R_2}\right]}\quad \left[\frac{V}{\sqrt{Hz}}\right]$$ Thermal noise of $R_1 \| R_2$

$$(4)\quad k_B = 1.38065\cdot 10^{-23}\quad \left[\frac{J}{K}\right]$$ Boltzmann Constant

$$(5)\quad T(K) = 237.15 + T(°C)\quad [\,K\,]$$ Temperature in kelvins

(B) Noise in Inverting Gain Configuration



Noise at the output is given as E_O, where

$$(6)\quad E_O = \left(1+\frac{R_2}{R_S+R_1}\right)\cdot\sqrt{(e_N)^2+\left(e_{R_1+R_S\|R_2}\right)^2+\left(i_N\cdot\left[\frac{(R_S+R_1)\cdot R_2}{R_S+R_1+R_2}\right]\right)^2}\quad [\,V_{RMS}\,]$$

$$(7)\quad e_{R_1+R_S\|R_2} = \sqrt{4\cdot k_B\cdot T(K)\cdot\left[\frac{(R_S+R_1)\cdot R_2}{R_S+R_1+R_2}\right]}\quad \left[\frac{V}{\sqrt{Hz}}\right]$$ Thermal noise of $(R_1 + R_S) \| R_2$

$$(8)\quad k_B = 1.38065\cdot 10^{-23}\quad \left[\frac{J}{K}\right]$$ Boltzmann Constant

$$(9)\quad T(K) = 237.15 + T(°C)\quad [\,K\,]$$ Temperature in kelvins

(1) e_N is the voltage noise of the amplifier. For the OPAx189 series of operational amplifiers, e_N = 5.8 nV / $\sqrt{Hz}$ at 1 kHz.
(2) i_N is the current noise of the amplifier. For the OPAx189 series of operational amplifiers, i_N = 165 fA / $\sqrt{Hz}$ at 1 kHz.
(3) For additional resources on noise calculations visit *TI's Precision Labs Series*.

Figure 9. Noise Calculation in Gain Configurations

ADVANCE INFORMATION

8.6 Device Functional Modes

The OPAx189 has a single functional mode, and is operational when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum power supply voltage for the OPAx189 is 36 V (±18 V).

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The OPAx189 operational amplifier combines precision offset and drift with excellent overall performance, making the series ideal for many precision applications. The precision offset drift of only 0.0035 µV/°C provides stability over the entire temperature range. In addition, the device pairs excellent CMRR, PSRR, and A_{OL} dc performance with outstanding low-noise operation. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

The following application examples highlight only a few of the circuits where the OPAx189 can be used.

9.2 Typical Applications

9.2.1 High-Side Voltage-to-Current (V-I) Converter

The circuit shown in Figure 10 is a high-side voltage-to-current (V-I) converter. The converter translates an input voltage of 0 V to 2 V into an output current of 0 mA to 100 mA. Figure 11 shows the measured transfer function for this circuit. The low offset voltage and offset drift of the OPAx189 facilitates excellent dc accuracy for the circuit.

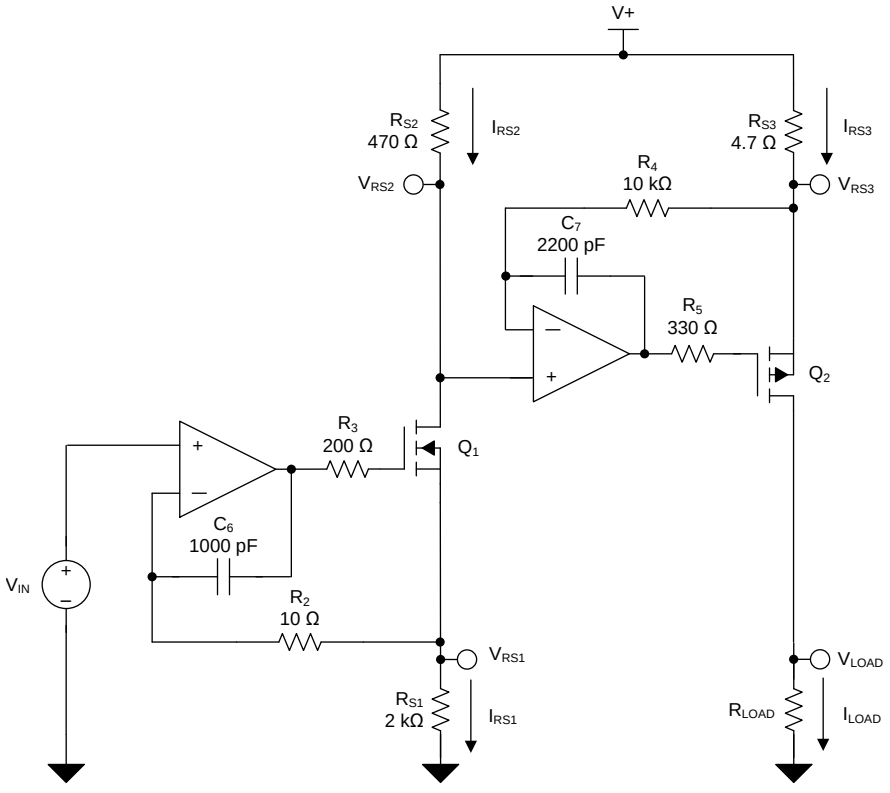


Figure 10. High-Side Voltage-to-Current (V-I) Converter

Typical Applications (continued)

9.2.1.1 Design Requirements

The design requirements are:

- Supply voltage: 5 V dc
- Input: 0 V to 2 V dc
- Output: 0 mA to 100 mA dc

9.2.1.2 Detailed Design Procedure

The V-I transfer function of the circuit is based on the relationship between the input voltage, V_{IN}, and the three current sensing resistors: R_{S1}, R_{S2}, and R_{S3}. The relationship between V_{IN} and R_{S1} determines the current that flows through the first stage of the design. The current gain from the first stage to the second stage is based on the relationship between R_{S2} and R_{S3}.

For a successful design, pay close attention to the dc characteristics of the operational amplifier chosen for the application. To meet the performance goals, this application benefits from an operational amplifier with low offset voltage, low temperature drift, and rail-to-rail output. The OPAx189 CMOS operational amplifier is a high-precision, ultra-low offset, ultra-low drift amplifier, optimized for low-voltage, single-supply operation, with an output swing to within 15 mV of the positive rail. The OPAx189 family uses chopping techniques to provide low initial offset voltage and near-zero drift over time and temperature. Low offset voltage and low drift reduce the offset error in the system, making this family appropriate for precise dc control. The rail-to-rail output stage of the OPAx189 makes sure that the output swing of the operational amplifier is able to fully control the gate of the MOSFET devices within the supply rails.

A detailed error analysis, design procedure, and additional measured results are given in reference design TIPD102, which is a step-by-step process to design a *High-Side Voltage-to-Current (V-I) Converter*.

TI Precision Designs

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, refer to TI Precision Design TIPD102, *High-Side Voltage-to-Current (V-I) Converter* (SLAU502).

9.2.1.3 Application Curves

Figure 11 shows the measured transfer function for the high-side voltage-to-current converter shown in Figure 10 .

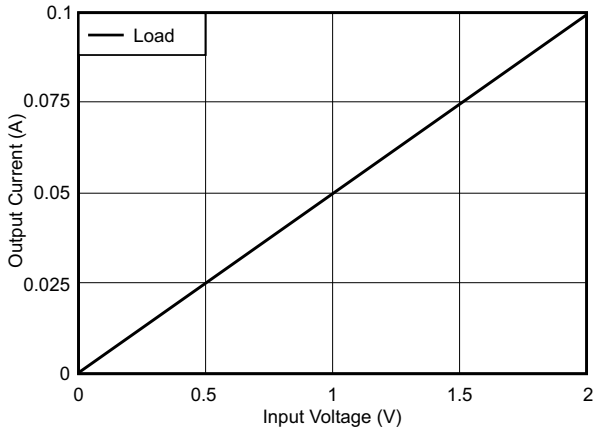


Figure 11. Measured Transfer Function for High-Side V-I Converter

ADVANCE INFORMATION

9.2.2 25-kHz Low-pass Filter

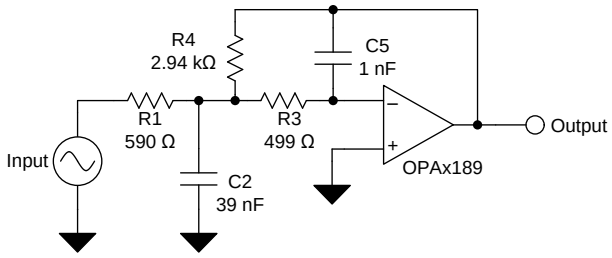


Figure 12. 25-kHz Low-pass Filter

9.2.2.1 Design Requirements

Low-pass filters are commonly employed in signal processing applications to reduce noise and prevent aliasing. The OPAx189 devices are ideally suited to construct high-speed, high-precision active filters. Figure 12 shows a second-order, low-pass filter commonly encountered in signal processing applications.

Use the following parameters for this design example:

- Gain = 5 V/V (inverting gain)
- Low-pass cutoff frequency = 25 kHz
- Second-order Chebyshev filter response with 3-dB gain peaking in the passband

9.2.2.2 Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in Figure 12. Use Equation 1 to calculate the voltage transfer function.

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1R_3C_2C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3R_4C_2C_5} \quad (1)$$

This circuit produces a signal inversion. For this circuit, the gain at DC and the low-pass cutoff frequency are calculated by Equation 2:

$$\text{Gain} = \frac{R_4}{R_1}$$

$$f_C = \frac{1}{2\pi}\sqrt{(1/R_3R_4C_2C_5)} \quad (2)$$

Software tools are readily available to simplify filter design. WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH® Filter Designer lets the user create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web based tool from the WEBENCH Design Center, WEBENCH Filter Designer allows board-level designers to create, optimize, and simulate complete multistage active filter solutions within minutes.

ADVANCE INFORMATION

9.2.2.3 Application Curve

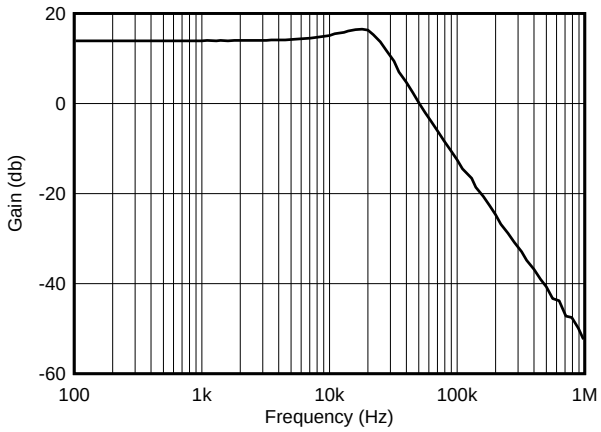


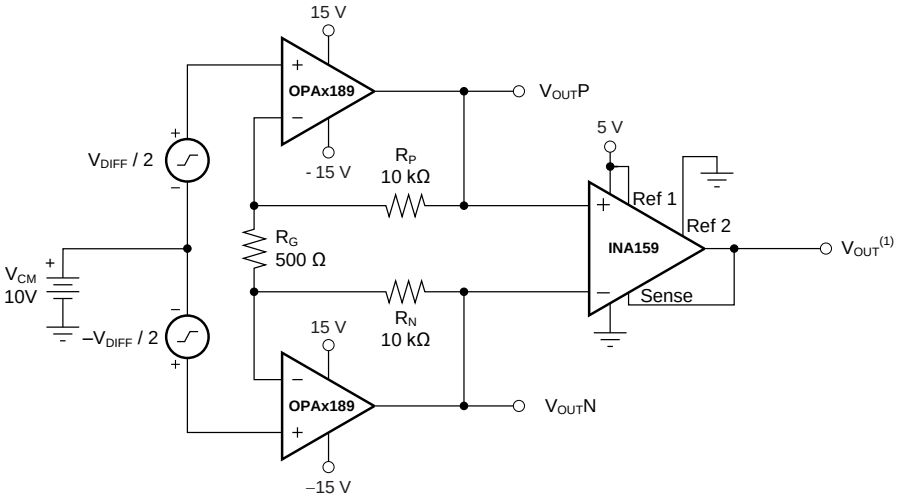
Figure 13. OPAx189 Second-Order, 25-kHz, Chebyshev, Low-Pass Filter

9.2.3 Discrete INA + Attenuation for ADC With 3.3-V Supply

NOTE

The TINA-TI files shown in the following sections require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

Figure 14 shows an example of how the OPAx189 is used as a high-voltage, high-impedance front-end for a precision, discrete instrumentation amplifier with attenuation. The INA159 provides the attenuation that allows this circuit to simply interface with 3.3-V or 5-V analog-to-digital converters (ADCs). Click the following link download the TINA-TI file: Discrete INA.



(1) $V_{OUT} = V_{DIFF} \times (41 / 5) + (Ref 1) / 2$.

Figure 14. Discrete INA + Attenuation for ADC With 3.3-V Supply

9.2.4 Bridge Amplifier

Figure 15 shows the basic configuration for a bridge amplifier. Click the following link to download the TINA-TI file: Bridge Amplifier Circuit.

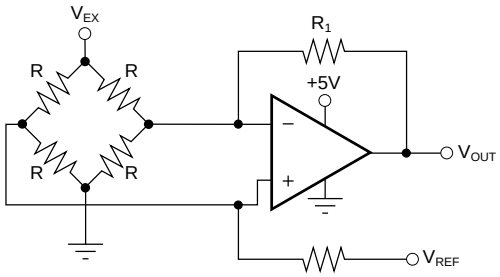


Figure 15. Bridge Amplifier

9.2.5 Low-Side Current Monitor

Figure 16 shows the OPAx189 configured in a low-side current-sensing application. The load current (I_{LOAD}) creates a voltage drop across the shunt resistor (R_{SHUNT}). This voltage is amplified by the OPAx189, with a gain of 201. The load current is set from 0 A to 500 mA, which corresponds to an output voltage range from 0 V to 10 V. The output range can be adjusted by changing the shunt resistor or gain of the configuration. Click the following link to download the TINA-TI file: Current-Sensing Circuit.

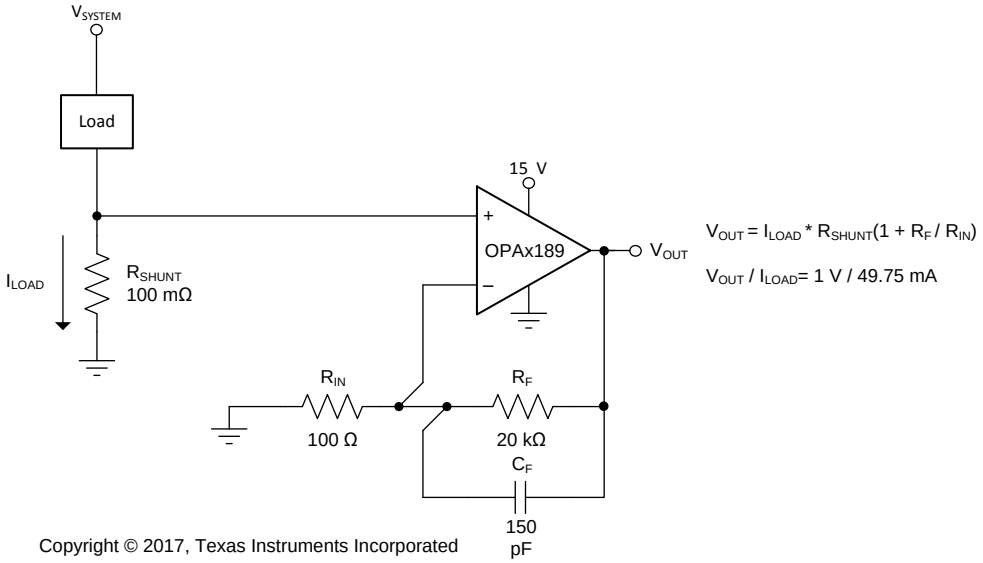


Figure 16. Low-Side Current Monitor

9.2.6 Programmable Power Supply

Figure 17 shows the OPAx189 configured as a precision programmable power supply using the 16-bit, voltage output DAC8581 and the OPA548 high-current amplifier. This application amplifies the digital-to-analog converter (DAC) voltage by a value of five, and handles a large variety of capacitive and current loads. The OPAx189 in the front-end provides precision and low drift across a wide range of inputs and conditions. Click the following link to download the TINA-TI file: Programmable Power-Supply Circuit.

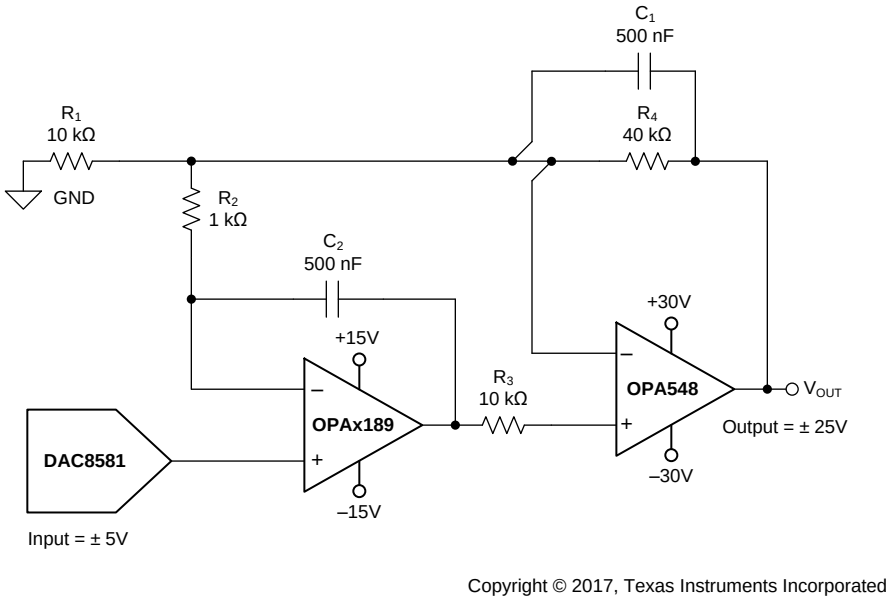
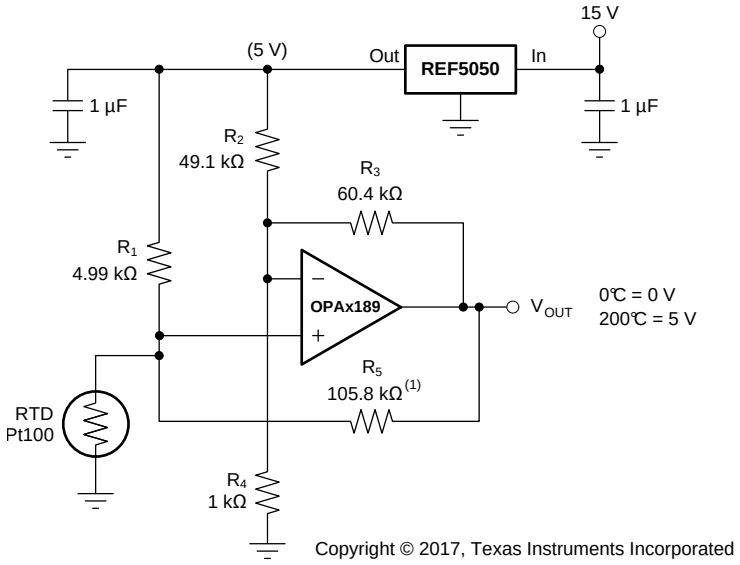


Figure 17. Programmable Power Supply

ADVANCE INFORMATION

9.2.7 RTD Amplifier With Linearization

See *Analog Linearization Of Resistance Temperature Detectors* (SLYT442) for an in-depth analysis of Figure 18. Click the following link to download the TINA-TI file: RTD Amplifier with Linearization.



(1) R_5 provides positive-varying excitation to linearize output.

Figure 18. RTD Amplifier With Linearization

ADVANCE INFORMATION

10 System Examples

10.1 24-Bit, Delta-Sigma, Differential Load Cell or Strain Gauge Sensor Signal Conditioning

OPAx189 is used in a 24-bit, differential load cell or strain gauge sensor signal conditioning system alongside the ADS1225. A pair of OPAx189 amplifiers are configured in a two-amp instrumentation amplifier (IA) configuration and are band-limited to reduce noise and allow heavy capacitive drive. The load cell is powered by an excitation voltage (denoted V_{EX}) of 5-V and provides a differential voltage proportional to force applied. The differential voltage can be quite small and both outputs are biased to V_{EX} / 2.

OPAx189 is employed here due to the excellent input offset voltage (0.4-µV) and input offset voltage drift (0.0035-µV/°C), the low broadband noise (5.8-nV/√Hz) and zero-flicker noise, and excellent linearity and high input impedance. The two-amp IA configuration removes the dc bias and amplifies the differential signal of interest and drives the 24-bit, delta-sigma ADS1225 analog-to-digital converter (ADC) for acquisition and conversion. The ADS1225 features a 100-SPS data rate, single-cycle settling, and simple conversion control with the dedicated START pin.

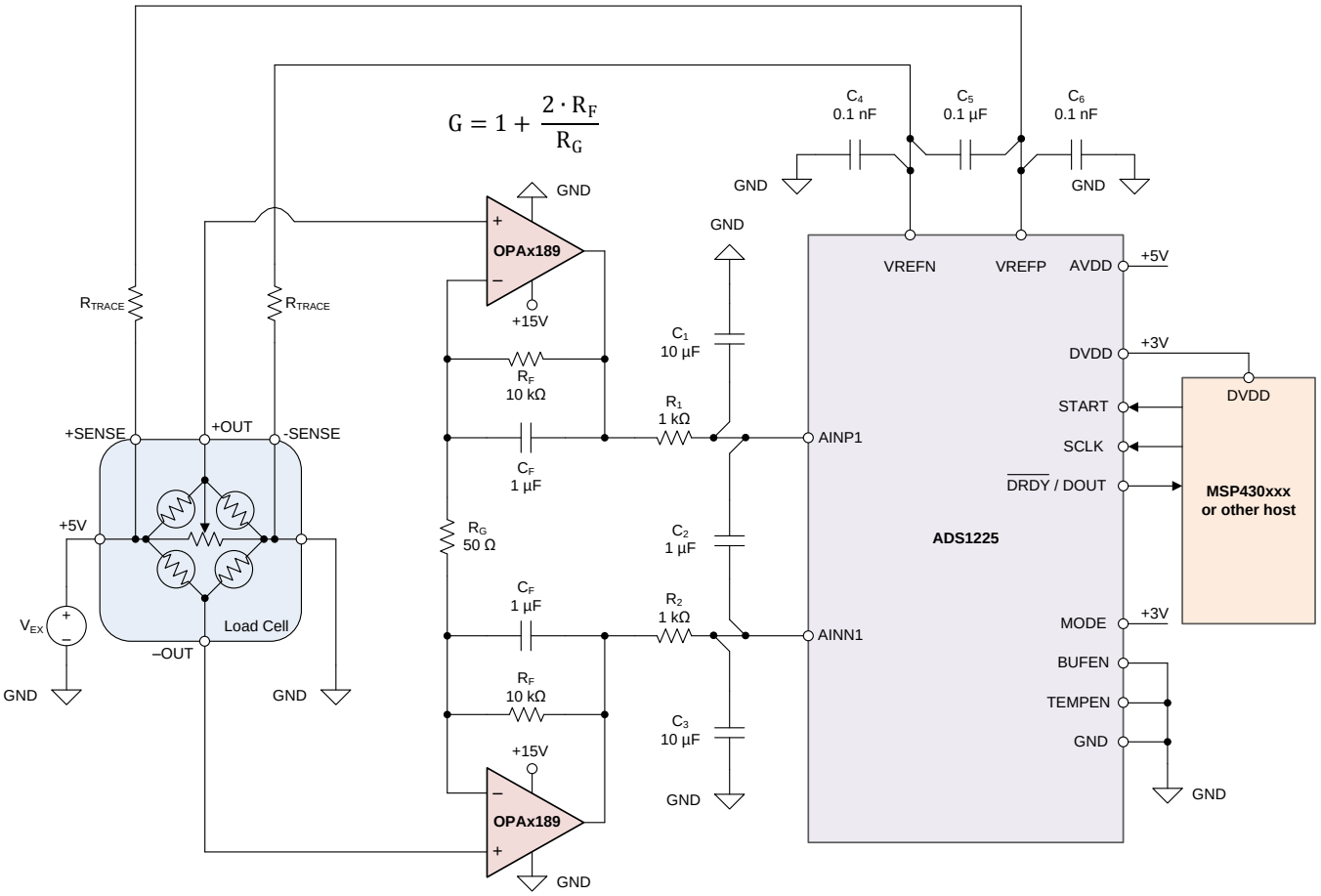


Figure 19. 24-Bit, Differential Load Cell or Strain Gauge Sensor Signal Conditioning Schematic

ADVANCE INFORMATION

11 Power Supply Recommendations

The OPAx189 is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to +125°C. The *Typical Characteristics* presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 40 V can permanently damage the device (see the *Absolute Maximum Ratings*).

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout* section.

12 Layout

12.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the op amp itself. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information, see *The PCB is a component of op amp design'*.
- To reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close as possible to the device. As illustrated in Figure 20, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- For best performance, TI recommends cleaning the PCB following board assembly.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, TI recommends baking the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

12.2 Layout Example

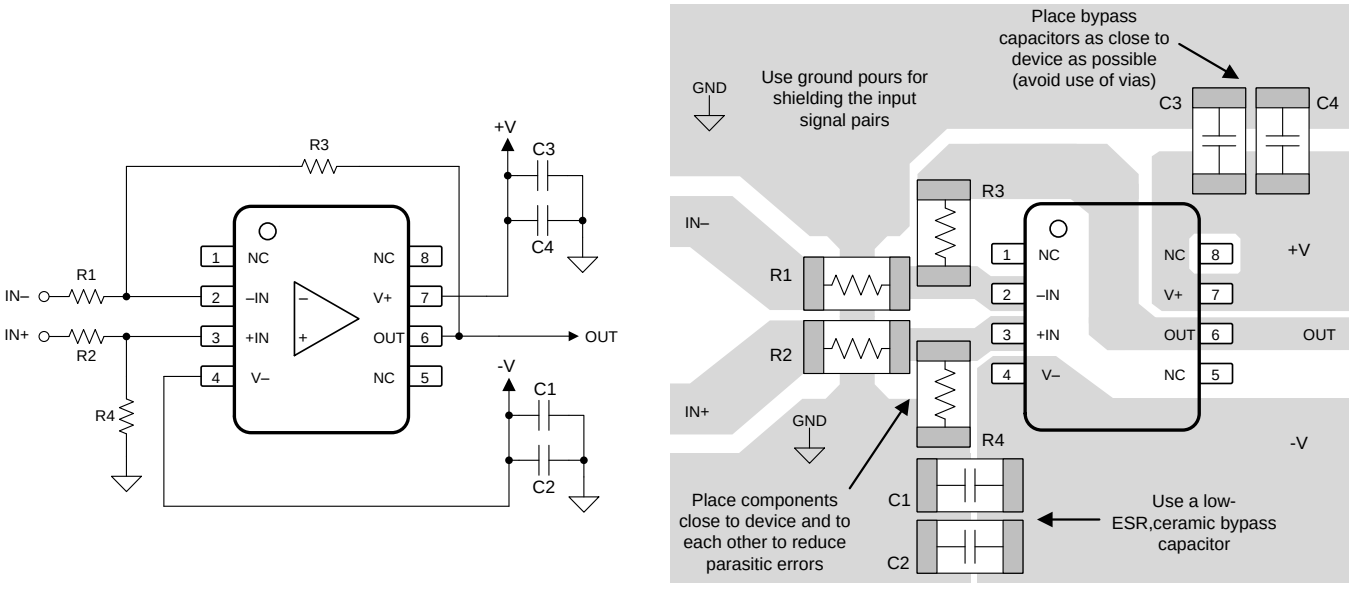


Figure 20. Operational Amplifier Board Layout for Difference Amplifier Configuration

13 Device and Documentation Support

13.1 Device Support

13.1.1 Development Support

13.1.1.1 TINA-TI™ (Free Software Download)

TINA-TI™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels in addition to a range of both passive and active models. TINA-TI™ provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI™ offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI™ software be installed. Download the free TINA-TI™ software from the TINA-TI™ folder.

13.1.1.2 TI Precision Designs

TI Precision Designs are available online at http://www.ti.com/ww/en/analog/precision-designs/. TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

13.2 Documentation Support

13.2.1 Related Documentation

For related documentation see the following:

- *Zero-drift Amplifiers: Features and Benefits* (SBOA182)
- *The PCB is a component of op amp design* (SLYT166)
- *Operational amplifier gain stability, Part 3: AC gain-error analysis* (SLTY383)
- *Operational amplifier gain stability, Part 2: DC gain-error analysis* (SLYT374)
- *Using infinite-gain, MFB filter topology in fully differential active filters* (SLYT343)
- *Op Amp Performance Analysis* (SBOA054)
- *Single-Supply Operation of Operational Amplifiers* (SBOA059)
- *Tuning in Amplifiers* (SBOA067)
- *Shelf-Life Evaluation of Lead-Free Component Finishes* (SZZA046)
- *Feedback Plots Define Op Amp AC Performance* (SBOA015)
- *EMI Rejection Ratio of Operational Amplifiers* (SBOA128)

13.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA189	Click here	Click here	Click here	Click here	Click here
OPA2189	Click here	Click here	Click here	Click here	Click here
OPA4189	Click here	Click here	Click here	Click here	Click here

ADVANCE INFORMATION

13.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.6 Trademarks

TINA-TI, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
Bluetooth is a registered trademark of Bluetooth SIG, Inc.
DesignSoft, TINA are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

13.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA189ID	PREVIEW	SOIC	D	8	75	TBD	Call TI	Call TI	-40 to 125		
OPA189IDR	PREVIEW	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125		
OPA2189ID	PREVIEW	SOIC	D	8	75	TBD	Call TI	Call TI	-40 to 125		
OPA2189IDGKR	PREVIEW	VSSOP	DGK	8	2500	TBD	Call TI	Call TI	-40 to 125		
OPA2189IDGKT	PREVIEW	VSSOP	DGK	8	250	TBD	Call TI	Call TI	-40 to 125		
OPA2189IDR	PREVIEW	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125		
POPA189ID	ACTIVE	SOIC	D	8	75	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

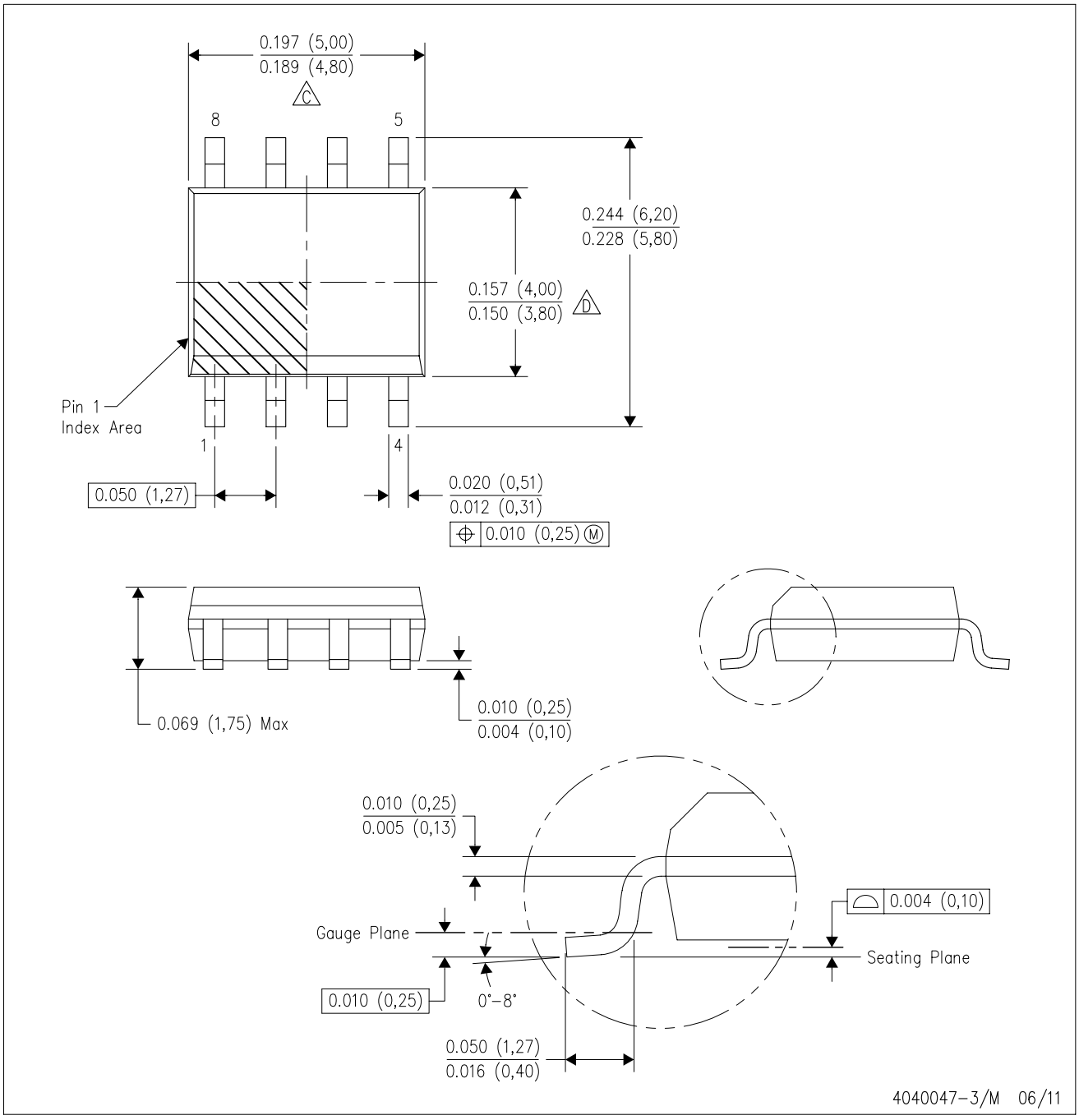
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

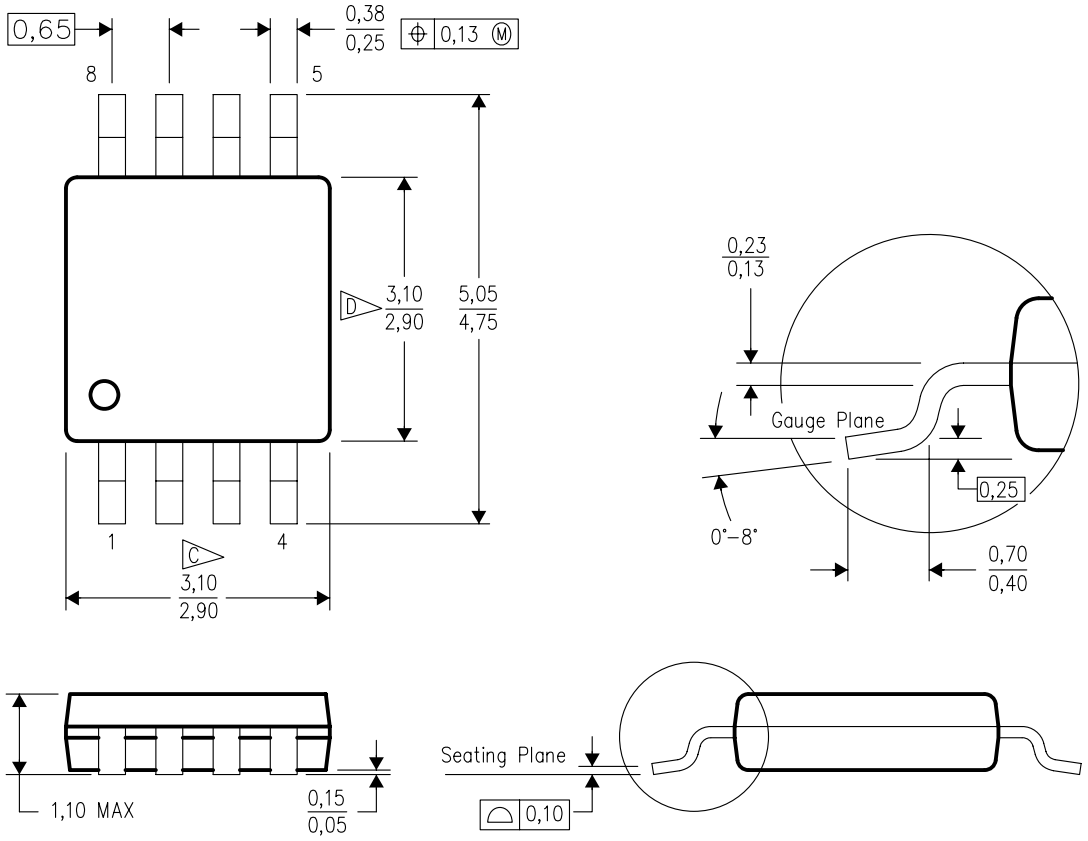
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265